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18EVE13

First Semester M.Tech. Degree Examination, Dec.2018/Jan.2019
Advanced Embedded System

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What are the different processors used in embedded system? **(04 Marks)**

b. Discuss I_2C communication interface with neat diagram. **(06 Marks)**

c. Explain role of watchdog timer in embedded system with relevant figure. **(04 Marks)**

d. Compare the following:
i) Big Endian and little Endian
ii) RISC and CISC
iii) Von-Neumann and Hardvard architecture **(06 Marks)**

OR

2 a. Explain operation of UART. Compare UART and USB. **(06 Marks)**

b. Compare PLD, ASIC and COTS. **(06 Marks)**

c. Discuss the operational and non-operational attributes of embedded system. **(08 Marks)**

Module-2

3 a. What is hardware software co-design? Explain fundamental issues in hardware-software co-design. **(06 Marks)**

b. Explain the difference between DFG and CDFG model. **(06 Marks)**

c. Design an automatic seat belt warning system based on FSM model and write relevant timer model. **(08 Marks)**

OR

4 a. Explain different firmware design approaches. **(06 Marks)**

b. Discuss the different techniques for embedding firmware into target board for a non-OS based embedded system. **(08 Marks)**

c. Explain In-circuit Emulator based debugging in detail. **(06 Marks)**

Module-3

5 a. List the architectural features of Cortex M3. **(06 Marks)**

b. Explain role of each registers and SFR in Cortex M3. **(08 Marks)**

c. Discuss features of NVIC. **(06 Marks)**

OR

6 a. With relevant diagram, explain operation modes of Cortex M3. **(08 Marks)**

b. What is 2-stack model in Cortex M3? Explain the role of control register. **(06 Marks)**

c. List the applications of ARM cortex M3. **(06 Marks)**

Module-4

7 a. Explain : (i) ASR.W (ii) LSL.W (iii) ROR.W (iv) LDR (v) ADR with examples. **(10 Marks)**

b. Describe bit band addressing with neat memory diagram. **(06 Marks)**

c. Explain three stage pipeline in ARM Cortex M3. **(04 Marks)**

OR

8 a. Differentiate CMP, CMN and TST instructions with example. (06 Marks)
b. With neat timing diagram, explain how data loss can be prevented with bit-band feature. (08 Marks)
c. Explain:
i) BFC.W R_d, R_n, #LSB, #width
ii) SXTB R_d, R_n
iii) STMIA R_d!, <reg> (06 Marks)

Module-5

9 a. Write a note on reasons for occurrence of following faults exceptions:
i) Bus
ii) Memory management
iii) Hard fault
iv) Usage fault (08 Marks)
b. Write an assembly program to find sum of 10 numbers from 1 to 10. (05 Marks)
c. Explain briefly SYSTICK along with registers. (07 Marks)

OR

10 a. Briefly explain how priorities are assigned to interrupts. (06 Marks)
b. What is CMSIS? List and explain CMSIS area of standardization. (06 Marks)
c. Explain role of:
i) Enable and clear enable registers
ii) Set pending and clear pending
iii) Priority level
iv) Active status (08 Marks)

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